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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,908	02/10/2004	Leonard Forbes	400.272US01	1212

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,908	FORBES, LEONARD	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 35-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 35-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 04/20/2006, which for some administrative technical details is not forwarded to the examiner's attention until 08/30/2006, has been reviewed and placed of record in the file.

2. Applicant's arguments with respect to amended claims 1 and 35-44, filed 04/20/2006, have been considered but they are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1 and 35-40** are rejected under 35 U.S.C. 102(e) as being anticipated by Tripsas et al. U.S. Patent 6,735,123 (hereinafter the '123 reference).

Referring to **claim 1**, the '123 reference discloses an NROM memory transistor (col. 1, lines 5-25, nitride-based "read only memory") comprising:

a substrate (21, Figs. 2 or 6o, col. 4, lines 1-15) having a plurality of source/drain regions (22/24), the source/drain regions having a different conductivity type than the remainder of the substrate (as is known in the art);

a nanolaminate gate dielectric (28/30/36, formed of a laminate of nano-thick layers 28, 30, and 36, col. 4, lines 40+) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric composed of oxide-nitride- HfO_2 (silicon dioxide –

silicon nitride – hafnium oxide HfO_2 , col. 4, lines 40-67) wherein the nitride layer (30) is a homogeneous nitride layer (col. 4, lines 52-60, and as could be appreciated from the figures); and

a control gate (38, col. 4, lines 10-15) formed on top of the gate dielectric.

Referring to **claims 35 and 37**, the reference further discloses that the plurality of source/drain regions are comprised of an n+ type doped silicon ("n-type doped" silicon) in the p-type silicon ("lightly doped" p-type) substrate (col. 4, lines 25-30).

Referring to **claim 36**, the reference further discloses that the control gate (38) is a polysilicon material (col. 4, lines 10-15).

Referring to **claims 38-40**, the limitations "fabricated using atomic layer deposition", "fabricated using an evaporation technique", and "fabricated using a combination of an atomic layer deposition and an evaporation technique" in the limitations "wherein the nanolaminate gate dielectric is fabricated using atomic layer deposition", "wherein the nanolaminate gate dielectric is fabricated using an evaporation technique", and "wherein the nanolaminate gate dielectric is fabricated using a combination of an atomic layer deposition and an evaporation technique" are taken to be product-by-process limitations and considered non-limitation in the product claims (MPEP 2112.01 and MPEP 2113). Specifically, in the instant case, differential characteristics of the claimed nanolaminate gate dielectric and the reference nanolaminate gate dielectric have not been positively claimed and established.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 41-44** are rejected under 35 U.S.C. §103(a) as being unpatentable over Tripsas et al. U.S. Patent 6,735,123 (the '123 reference).

Referring to **claims 41 and 44**, the '123 reference discloses an NROM memory transistor as claimed and as detailed above for claim 1, but does not teach that the NROM memory transistor could be formed in a memory array including an array of the NROM memory transistors, and further does not teach that the memory array could be used in an electronic system including a processor and a memory device. However, as the reference also does not exclude such usage, such utilization of the NROM memory transistor in an array and eventually in an electronic system would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claim 42**, the reference further discloses that the pair of source/drain regions are n+ doped regions in a p-type substrate, as noted above for claims 35 and 37.

Referring to **claim 43**, the reference further discloses, as noted above for claims 36 and 37, that the substrate is silicon and the control gate is polysilicon.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 7:30 am - 6:00 pm, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
September 01, 2006